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INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>		Application Number	09/844,670
		Filing Date	April 30, 2001
		First Named Inventor	THEKKATH
		Group Art Unit	2124 2193
		Examiner Name	Anil KHATRI
Sheet	1 of 1	Attorney Docket Number	MTEC-011/00US

FOREIGN PATENT DOCUMENTS

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✓	D1	Susan J. EGGERS, et al., "Techniques for Efficient Inline Tracing on a Shared-Memory Multiprocessor," University of Washington, 1990 ACM, pp. 37-47.	
✓	D2	Richard A. UHLIG, et al., "Trace-Driven Memory Simulation: A Survey," Intel Microcomputer Research Lab; University of Michigan, <i>ACM Computing Surveys</i> , Vol. 29, No. 2, June 1997, pp. 128-170.	
✓	D3	Eric ROTENBERG, et al., "Trace Processors," University of Wisconsin, 1997 <i>IEEE Service Center</i> , 12 pp.	
✓	D4	E.N. ELNOZAHY, "Address Trace Compression Through Loop Detection and Reduction," ©1999 ACM I-58113-083, pp. 214, 215.	
✓	D5	Darren JONES, "Opal Coprocessor Interface," <i>MIP Proprietary/Confidential</i> , June 4, 1999, pp. 1-18.	
✓	D6	Darren JONES, <i>MIPSS64™ SKC™ Processor Cores User's Manual</i> , Rev. 1.0, July 4, 1999, pp. 6-1 to 6-26.	
✓	D7	<i>MIPSS64™ SKC™ Processor Cores User's Manual</i> , Rev. 1.0.1., 1999, pp. 247-276.	

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